

S P E C I F I C A T I O N

Docket No. 92-C-74

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN that I, Frank Randolph Bryant, citizen of the United States of America, residing in the State of Texas, have invented new and useful improvements in a

TRANSISTOR STRUCTURE AND METHOD FOR MAKING SAME

of which the following is a specification:

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1 BACKGROUND OF THE INVENTION

2 1. Field of the Invention:

3 The present invention relates to integrated circuit
4 devices and more specifically to field effect devices such
5 as field effect transistors (FET) for use in integrated
6 circuits.

7 2. Description of the Prior Art:

8 In manufacturing transistors, re-oxidation has been
9 used in 5 μm to 1.2 μm technologies to improve transistor
10 lifetimes and gate oxide reliability due to higher fields
11 occurring at the etched polysilicon transistor edges. For
12 example, U.S. Patent No. 4,553,314 teaches using re-
13 oxidation to manufacture semiconductor devices. Typically,
14 3 μm and 5 μm technologies use re-oxidation thicknesses
15 from about 1200 \AA to about 2500 \AA depending on the
16 particular device. In 1.5 μm and 2 μm technologies, re-
17 oxidation thicknesses from about 500 \AA to about 1,000 \AA are
18 used.

19 In 0.8 μm technology, however, the re-oxidation
20 process has been discontinued because the lifetimes of
21 transistors currently manufactured without the re-oxidation
22 process is better than with the re-oxidation process. Such
23 a situation is caused by the formation of asperities on the
24 underside of the polysilicon layer of the transistor during
25 the re-oxidation process. These asperities are of little
26 importance until the gate oxide thicknesses are reduced to
27 below 200 \AA as used in submicron technology. At this
28 point, the asperities become a contributor to the increased
29 field at the transistor edge and of hot carrier injection
30 (HCI). These asperities are caused by (1) oxidant
31 diffusion along polysilicon grain boundaries creating
32 single crystal silicon protrusions and (2) oxide
33 thicknesses under the polysilicon edge increasing during
34 re-oxidation, causing polysilicon grain boundary slip to

1 occur and creating multiple edges, which results in an
2 overall increase in angle geometries.

3 In addition, moving to device geometries below 0.8 μm
4 technology has resulted in marginal lifetimes of the
5 transistors. Thus, it is desirable to have a gate
6 structure that has an increased lifetime using re-oxidation
7 under the gate edge but without the asperities caused by
8 presently used re-oxidation processes.

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1 SUMMARY OF THE INVENTION

2 The present invention is a gate structure in a
3 transistor and method for fabricating the structure. A
4 gate structure is formed on a substrate. The gate
5 structure includes three layers: an oxide layer, a nitride
6 layer and a polysilicon layer. The oxide layer is located
7 on the substrate, the nitride layer is located on the oxide
8 layer, and the polysilicon layer is located on the nitride
9 layer. The gate structure is reoxidized to form a layer of
10 oxide over the gate structure. The nitride layer prevents
11 the formation of asperities on the underside of the
12 polysilicon layer during reoxidation of the transistor.

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1 BRIEF DESCRIPTION OF THE DRAWINGS

2 The novel features believed characteristic of the
3 invention are set forth in the appended claims. The
4 invention itself however, as well as a preferred mode of
5 use, and further objects and advantages thereof, will best
6 be understood by reference to the following detailed
7 description of an illustrative embodiment when read in
8 conjunction with the accompanying drawings, wherein:

9 Figures 1-4 illustrate cross-sections of a portion of a
10 semiconductor device during fabrication;

11 Figure 5 illustrates a cross-section of a semiconductor
12 device;

13 Figure 6 illustrates a semiconductor device after
14 reoxidation;

15 Figures 7A-7C depict an enlarged view of the cross-section
16 shown in Figure 5;

17 Figure 8 illustrates an enlarged view of a cross-section
18 from Figure 6;

19 Figures 9-10 illustrate cross-sections of a portion of a
20 semiconductor device during an implantation process;

21 Figure 11 depicts a cross-section of a semiconductor device
22 after reoxidation and implantation of the source and drain
23 regions; and

24 Figure 12 is a graph of current injection for two
25 semiconductor devices.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. The figures representing cross-sections of portions of an integrated circuit during fabrication are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

The present invention allows for the use of re-oxidation to improve transistor lifetimes by reducing fields in transistor technologies through elimination of previous limitations. According to the present invention, a structure is provided which uses the increased distance at the gate edge, but eliminates the asperities created during re-oxidation so that re-oxidation may be used for submicron technologies. The structure of the present invention prevents the effects of oxidation on the polysilicon gate by using a thin silicon nitride layer located between the polysilicon and the gate oxide in a transistor.

Referring now to Figure 1, a schematic cross-section of a semiconductor device at an early stage in a manufacturing process is illustrated according to the present invention. Transistor 10 includes a substrate 12, which is typically a monocrystalline silicon of a conventional crystal orientation known in the art. Many features of the present invention are applicable to devices employing semiconductor materials other than silicon as will be appreciated by those of ordinary skill in the art. Substrate 12 may be either a p-type substrate or an n-type

1 substrate. In the present illustrative example, a p-type
2 substrate is employed. As can be seen with reference to
3 Figure 1, field oxides 14a and 14b have already been
4 created in transistor 10.

5 In Figure 2, oxide layer 16, also called an insulating
6 oxide layer or a gate oxide layer, is grown on surface 18
7 of substrate 12 in transistor 10. Thereafter, in Figure 3,
8 a silicon nitride layer 20 is deposited on top of oxide
9 layer 16 and field oxide 14a and 14b. Silicon nitride
10 layer 20 is deposited on transistor 10 in a layer that is
11 preferably from about 10 Å to about 50 Å thick according to
12 the present invention.

13 Thereafter, a polycrystalline silicon (polysilicon)
14 layer 22 is deposited over silicon nitride layer 20 as
15 illustrated in Figure 4. Alternatively, a refractory
16 metal, such as Mo, Ta, or W, or a metal silicide, such as
17 MoSi_2 , TaSi_2 , or WSi_2 , may be used. Transistor 10 is then
18 patterned and etched to expose surface 18 in selected
19 portions of transistor 10 as illustrated in Figure 5
20 wherein a gate structure 21 for transistor 10 is formed.
21 Next, re-oxidation is performed to produce oxide layer 26
22 covering the gate structure and the substrate, as
23 illustrated in Figure 6. Typically, in reoxidation, the
24 exposed substrate and the gate structure are exposed to an
25 oxidizing ambient. Such a process is well known to those
26 skilled in the art. Also, oxide layer 26 produced by
27 reoxidation is preferably from about 25 Å to about 500 Å
28 thick on the p-type substrate.

29 Referring now to Figure 7, an enlarged view of a
30 representative portion of Figure 5 is depicted. The figure
31 shows in greater detail a portion of gate 21. As can be
32 seen, polysilicon layer 22, nitride layer 20, and oxide
33 layer 16 have been etched away to expose surface 18 of
34 substrate 12. Alternatively, oxide layer 16 may be left in

1 its entirety as illustrated in Figure 7B, or partially
2 etched away as illustrated in Figure 7C.

3 Now referring to Figure 8, an enlarged view of
4 transistor 10 from Figure 6 is depicted. This enlarged
5 view shows oxide layer 26 as grown during reoxidation of
6 transistor 10. The reoxidation process which results in
7 the growth of oxide layer 26 has the effect of moving
8 peripheral edge 40 of polysilicon layer 22 in gate
9 structure 21, as illustrated in Figure 8. The position of
10 the peripheral edge of gate structure 21 in polysilicon
11 layer 22 is indicated by the dashed line 40'. In addition,
12 the growth of oxide layer 26 moves surface 18 downward from
13 its original position 18' to form an indentation 19 (the
14 section of oxide from original position 18' to surface 18)
15 in surface 18 of substrate 12 near the peripheral edge of
16 gate structure 21. Also, nitride layer 20 has an uplift
17 20a caused by reoxidation of the transistor.

18 The reoxidation process is well to those skilled in
19 the art. Various temperatures and times may be used
20 depending on the oxidizing ambient employed. For example,
21 the transistor may be exposed to an oxidizing ambient such
22 as dilute steam at a temperature from about 650°C to about
23 900°C from about 10 minutes to about 60 minutes.

24 Nitride layer 20 acts as a protective layer and
25 prevents the formation of asperities in polysilicon layer
26 22 in gate structure 21 during reoxidation. Nitride layer
27 20 prevents oxidation of the bottom side of the polysilicon
28 layer 22 and prevents formation of geometries which result
29 in increased electric fields. In addition, the nitride
30 layer will prevent outdiffusion of polysilicon dopants into
31 the gate oxide, which if excessive can lead to early gate
32 break downs. Such a feature is important especially when
33 polysilicon dopants such as boron are used in large
34 amounts. Moreover the higher density silicon nitride

1 increases resistance of the gate oxide to physical damage
2 during post gate oxide and polysilicon deposition
3 silicidations.

4 Although the process depicted in Figures 1-4 deposits
5 silicon nitride onto the gate oxide layer, other processes
6 may be employed to create a silicon nitride layer between
7 gate oxide layer 16 and the polysilicon layer 22. For
8 example, a nitrogen (N_2) implant into the polysilicon
9 followed by annealing the device forms a thin silicon
10 nitride layer at the polysilicon oxide interface. More
11 information on forming thin silicon nitride layers may be
12 found in an article by Josquih et al., "The Oxidation
13 Inhibition in Nitrogen Implanted Silicon", J. Electrochem.
14 Soc: SOLID-STATE SCIENCE AND TECHNOLOGY (August 1982) pp.
15 1803-1811 and in United States Patent No. 5,250,456.

16 When nitrogen implantation is used to form a silicon
17 nitride layer, polysilicon layer 22 is deposited over oxide
18 layer 16 as illustrated in Figure 9. Thereafter, nitrogen
19 ions are implanted into transistor 10 as illustrated in
20 Figure 10. In accordance with a preferred embodiment of
21 the present invention, $^{15}N_2^+$ at a dose in the range of about
22 $1E14$ to $1E16$ ions/cm². Thereafter, transistor 10 is
23 annealed at a temperature from about 800°C to about 1100°C
24 inert ambient gas, such as ~~argon or~~ helium, for about 15
25 minutes to 60 minutes. As a result, a nitride layer 20 as
26 illustrated in Figure 4 results from the annealing process.
27 Nitride layer 20 is formed in a layer from about 15 Å to
28 about 20 Å thick. Alternatively, transistor 10 may be
29 annealed using rapid thermal processing in an inert ambient
30 gas at about 900°C to about 1200°C for a period of time
31 from about 5 seconds to about 3 minutes.

32 The anneal of the nitrogen-implanted polysilicon
33 overlying oxide layer 16 causes the implanted nitrogen to
34 accumulate at the polysilicon/oxide interface, forming a

1 nitride layer. Thereafter, transistor 10 is patterned and
2 etched as illustrated in Figure 5 and re-oxidized as shown
3 in Figure 6.

4 Alternatively, silicon nitride layer 20 may be formed
5 on top of oxide layer 16, as illustrated in Figure 3, using
6 a rapid thermal anneal process. For example, N_2 or NH_3 may
7 be employed in a rapid thermal anneal process at a
8 temperature from about 700°C to about 1200°C for a period
9 of time from about 10 seconds to about 300 seconds to form
10 a silicon nitride layer.

11 Implantation to produce source and drains for
12 transistor 10 may performed after the re-oxidation
13 procedure as illustrated in Figure 11. For example, n-type
14 impurities may be implanted into a p-type substrate. The
15 source/drain regions 30a and 30b are n-type active regions.
16 Lightly doped drain (LDD) regions 32a and 32b are defined
17 using sidewall oxide spacers 36a and 36b as known by those
18 skilled in the art. The processing employed to produce the
19 additional structures described in Figure 10 after
20 reoxidation are well known to those skilled in the art.
21 Alternatively, LDDs 32a and 32b and sidewall spacers 36a
22 and 36b may be omitted according to the present invention.

23 Referring now to Figure 12, a graph of current
24 injection for two semiconductor devices is depicted. The
25 graph is of injection current, IG, for different voltages.
26 IG currents for a first semiconductor without a nitride
27 layer located between the polysilicon gate and the gate
28 oxide is represented by line 1. IG currents for a second
29 semiconductor device including a nitride layer between the
30 polysilicon and gate oxide is represented by line 2. As
31 can be seen from the graph in Figure 12, the early rise
32 currents are reduced in line 2. The two semiconductor
33 devices are both n-channel transistors with oxide spacers.
34 The two devices have a 0.7 μm wide gate finger structure

1 and area of about $2e^4 \mu m^2$. Both devices under went
2 reoxidation using $15 O_2$ at $800^\circ C$. The second device has a
3 nitride layer that is 10 \AA . Otherwise the first and second
4 devices are substantially identical. The nitride layer in
5 the second semiconductor device represented in line 2 was
6 created by silicon nitride deposition using a 30 minute
7 deposition time at $750^\circ C$. The second semiconductor device
8 was exposed to dichlorosilane ($SiCl_2H_2$) and ammonia (NH_3) in
9 a ratio of 1 part dichlorosilane to 10 parts ammonia.

10 While the invention has been particularly shown and
11 described with reference to a preferred embodiment, it will
12 be understood by those skilled in the art that various
13 changes in form and detail may be made therein without
14 departing from the spirit and scope of the invention.

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